Your Comments Please

HP E2434B

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
2. Were you satisfied with the operation of the product at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

If not, what was missing?

Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this product be used to make?_____

_____.

5. Which logic analyzer are you using?

Type_____

6. What do you like most about the product? _____

_____

7. What would you like to see changed or improved?_____

8. Which sections of the manual(s) have you used?

[ ] Installation Overview
[ ] Step-By-Step Procedures
[ ] Characteristics

9. Please rate the manual(s) on the following:

4= Excellent 3= Good 2= Adequate 1= Poor

[ ] Breadth and depth of information
[ ] Ability to easily find information
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Please explain:_____

10. What is your experience with logic analyzers?

[ ] No previous experience
[ ] Less than 1 year experience
[ ] More than 1 year's experience on one model
[ ] More than 1 year's experience on several models

Name _____ Company _____

Address _____ Zip Code _____

Phone _____ Instrument Serial # _____

THANK YOU FOR YOUR HELP

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Hiermit wird bescheinigt, daß das Gerät/System

HP 1650A/B and HP 1651A/B

in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation für Meß- und Testgeräte

Werden Meß- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Meßaufbauten verwendet, so ist vom Betreiber sicherzustellen, daß die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that this product HP 1650A/B and HP 1651A/B meets the radio frequency interference requirements of directive Vfg. 1046/84. The German Bundespost has been notified that this equipment was put into circulation and was granted the right to check the product type for compliance with these requirements.

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Note: This declaration indicates compliance of this product with the German RFI specifications stated in the German Vfg. 1046/84 directive.

HP E2434B
Intel 80C186EB/188EB
Preprocessor Interface
User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

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A software code may be printed after the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

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List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages	**Effective Date**

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This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Chapter 3: General Information

Appendix A: Troubleshooting

Introduction

This user's guide includes information on using the HP E2434B Preprocessor Interface to do logic analysis on the 80C186EB and 80C188EB microprocessors. All mention of 80C186EB in this user's guide collectively refers to both the 80C186EB and 80C188EB microprocessors, unless specifically noted otherwise. The HP E2434B Preprocessor Interface provides a complete interface between any Intel 80C186EB target system and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A.

There are additional connectors on the preprocessor interface which do not have active circuitry between the microprocessor and the logic analyzer. Since they do not add skew to the signals, the preprocessor interface can be used for timing analysis as well as state analysis.

The HP E2434B configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80C186EB microprocessor. It also loads an inverse assembler for obtaining displays of microprocessor data in the assembly language mnemonics of the microprocessor.

Logic Analyzer Software Compatibility

The HP E2434B Preprocessor Interface requires HP 16500B system software version V01.02 or higher; for the HP 16500A frame, version V06.00 is required. For the HP 1660A Logic Analyzer, software version V01.00 or higher is required. To use the enhanced inverse assembler with the HP 1660A Logic Analyzer, software version V02.00 or higher is required.

If your software version is older than those listed above, load new system software with a version number equal to or higher than those listed above before loading the HP E2434B software.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2434B Preprocessor Interface:

HP 1650A

This logic analyzer provides 1 k of memory depth with either 80 channels of 25 MHz state analysis or 80 channels of 100 MHz timing analysis. The HP 1650A Logic Analyzer requires HP 1650A system software version V1.11 or higher to operate with the HP E2434B Preprocessor Interface. If your HP 1650A software version is older than V1.11, load new HP 1650A software (V1.11 or higher) before loading the HP E2434B software.

HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 1660A/61A/62A

The HP 1660A/61A/62A Logic Analyzers provides 4 k of memory depth with 136 channels (HP 1660A), 102 channels (HP 1661A), or 68 channels (HP 1662A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with up to either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16542A (three cards)

This logic analyzer combination provides 1 M of memory depth with 48 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2434B Preprocessor Interface to perform measurements with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2434B software. It also provides information about the inverse assemblers and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2434B Preprocessor Interface.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2434B

Introduction

This chapter explains how to install and configure the HP E2434B Preprocessor Interface to perform measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2434B software, make a duplicate copy of the HP E2434B master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The HP E2434B Preprocessor Interface consists of the following:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The configuration files and inverse assembler software on a 3.5-inch disk.
- This user's guide.
- One PGA to PLCC Adapter (HP part number 1200-1752).
- One PLCC to PGA Socket (HP part number 1200-1751).
- Additional pin protectors (HP part numbers 1200-1744).

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with a protective foam pad. This is done to protect the delicate gold plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam protector.

Minimum Equipment Required

The minimum equipment required for analysis of 80C186EB target systems consists of the following items:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A (three cards), or HP 16550A Logic Analyzer. The HP 1650A Logic Analyzer requires HP 1650A system software version V1.11 or higher to operate with the HP E2434B.
- The HP E2434B Preprocessor Interface.
- HP E2434B option 1CC, for 80C186EB/188EB QFP target systems. QFP target systems also require a PLCC microprocessor.
- Additional pin protectors.

For 80C186EB/188EB QFP target systems, you must specify Option 1CC when ordering the HP E2434B, in order to receive the adapter. Without the adapter, the preprocessor interface will only work with PLCC target systems.

Note 

The above equipment is the minimum required for three-pod state analysis. There are seven additional connectors on the preprocessor interface which can be used for timing analysis. The seven additional connectors require either the General Purpose Probes shipped with your logic analyzer, or one 100 kOhm Termination Adapter per connector (HP part number 01650-63203).

Installation Overview

The following procedure describes the major steps required to perform measurements with the HP E2434B Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

1. Install the preprocessor interface on the target system (see page 1-6 or 1-9, depending on the microprocessor package).
2. Plug the logic analyzer pods into the preprocessor interface as shown in table 1-1 on page 1-11 (state) or table 1-2 on page 1-12 (timing). The 2 x 20-pin wide connectors do not require termination adapters. For pods P2, P5, P6, P7, and the Timing P4, connect 100 kOhm Termination Adapters (see page 1-13), or use the General Purpose (GP) probes shipped with your logic analyzer.
3. Load the logic analyzer configuration and inverse assembler by loading the appropriate file from the disk (see page 1-14).
4. If the capacitance from extenders interferes with the proper operation of the target system crystal or oscillator, install a crystal or oscillator on the preprocessor interface (see page 1-17).

You are now ready to make measurements with the logic analyzer. The rest of this chapter contains more detailed information on setting up the hardware and software.

Note

Some of the no-connect pins (NC) are not shielded, and may occasionally show activity. This activity does not affect the operation of the preprocessor interface or inverse assembler.

Attention! 

The Attention! symbol is used to indicate areas which might easily be overlooked, causing unexpected results. The Attention! symbol is used on several places on the signal labels which mount over the preprocessor interface. For a complete description of the areas which are marked with Attention! see page 1-15.

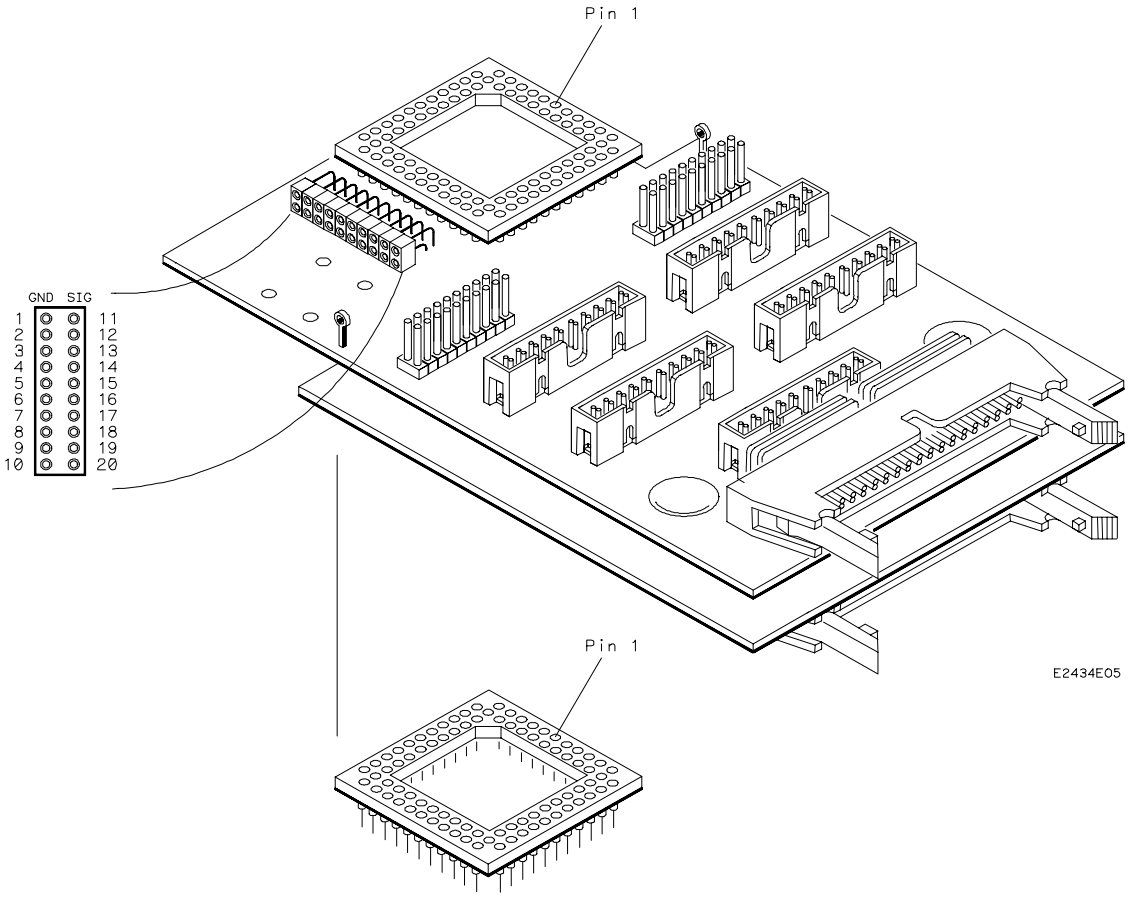

Figure 1-1. Preprocessor Interface

Caution

Care must be used when removing a microprocessor from the preprocessor interface board to prevent damaging the circuit traces.

Connecting to the Target System

The HP E2434B Preprocessor Interface can be used with PLCC or QFP target systems. PLCC systems require the PGA to PLCC Adapter, which is provided with the preprocessor interface; QFP target systems require HP E2434B option 1CC, which includes the *QFP Surface Mount Adapter Operating Note*. The HP E2434B Preprocessor Interface does not support 80C186EB/188EB PGA target systems; attempts to use the 80C186EB/188EB PGA microprocessor with the HP E2434B will result in damage. The following sections describe the connections:

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

Connecting to PLCC Target Systems

The PGA to PLCC Adapter is designed to plug into a standard PLCC socket assembly. Figure 1-2 shows the mapping of the PLCC pins onto the PGA socket of the preprocessor interface. To connect the preprocessor interface to a PLCC target system:

1. Using a PLCC extractor tool, remove the 80C186EB PLCC microprocessor from the microprocessor socket on the target system.

Caution 

Be careful not to damage the PLCC socket or microprocessor when removing the microprocessor from the socket.

2. Store the microprocessor in a protected environment.
3. Noting the position of pin 1, place the PGA to PLCC Adapter in the microprocessor socket on the target system (see figure 1-3).

Caution 

Serious damage to the target system or preprocessor interface can result from incorrect connection. Take care to note the position of pin 1 on the preprocessor interface, PGA to PLCC Adapter, and target system socket prior to inserting the connector in the socket. Also, take care that all microprocessor pins are making contact.

4. Connect the preprocessor interface PGA probe to the PGA socket on the PGA to PLCC Adapter.

Note If the preprocessor interface connector interferes with components of the target system, or if a higher profile is required, additional plastic pin protectors can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1744. However, any 84-pin PGA IC socket with the preprocessor interface's footprint and gold-plated pins can be used (see figure below).

---

5. Note the position of pin 1, and install the PLCC Socket in the PGA socket on the top of the preprocessor interface. Then install the PLCC-style 80C186EB microprocessor in the PLCC socket, ensuring that pin 1 is properly aligned (see figure 1-3).

Note For PLCC style microprocessors, the PLCC socket adds capacitance to the circuit, but should not affect microprocessor performance.

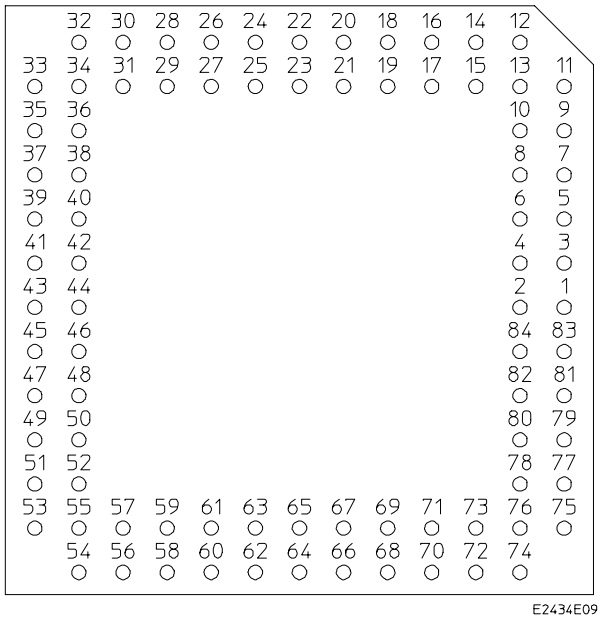

Figure 1-2. PGA to PLCC Pin Mapping (Top View)

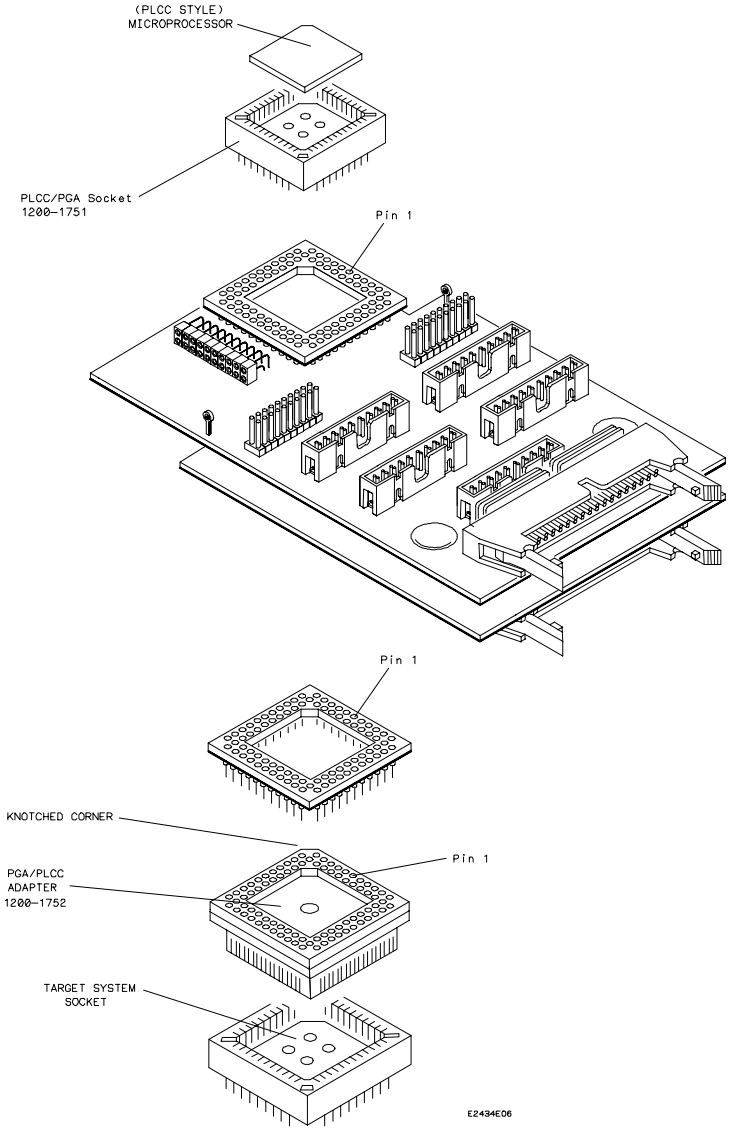

Figure 1-3. Connecting to a PLCC Socket

Caution 

The weight of the preprocessor interface can apply enough force to disconnect the PGA to PLCC Adapter. To prevent accidental disconnections, support the preprocessor interface in a stable position.

Connecting to QFP Target Systems

80C186EB QFP target systems require HP E2434B option 1CC, which includes the *QFP Surface Mount Adapter Assembly Operating Note*. To connect the preprocessor interface to a QFP target system, use the following procedure:

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

---

1. Using the directions in the *QFP Surface Mount Adapter Assembly Operating Note*, connect the adapter to the target system. Ensure that pin 1 is properly aligned.

Caution 

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 on the adapter and the target system socket prior to making connections. Also, take care to align the connectors so that all pins are making contact.

---

2. Plug the preprocessor interface into the PGA Transition Socket on the adapter, noting the position of pin 1 (see figure 1-1). There is a notch on the socket indicating pin 1.

Note 

If the preprocessor interface connector interferes with components of the target system, or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1744. However, any 84-pin PGA IC socket with the preprocessor interface's footprint and gold-plated pins can be used.

---

3. Note the position of pin 1, and install the PLCC to PGA Socket in the PGA socket on the top of the preprocessor interface. Then install the PLCC-style 80C186EB microprocessor in the PLCC socket, ensuring that pin 1 is properly aligned (see figure 1-3). The PLCC to PGA Adapter adds capacitance to the circuit, but should not affect microprocessor performance.

Connecting to the HP E2434B

Connect the logic analyzer cables to the preprocessor interface as shown in the following tables. Table 1-1 is for state analysis, and table 1-2 is for timing analysis. Designations such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod. Figure 1-4 shows the relative locations for the logic analyzer cards.

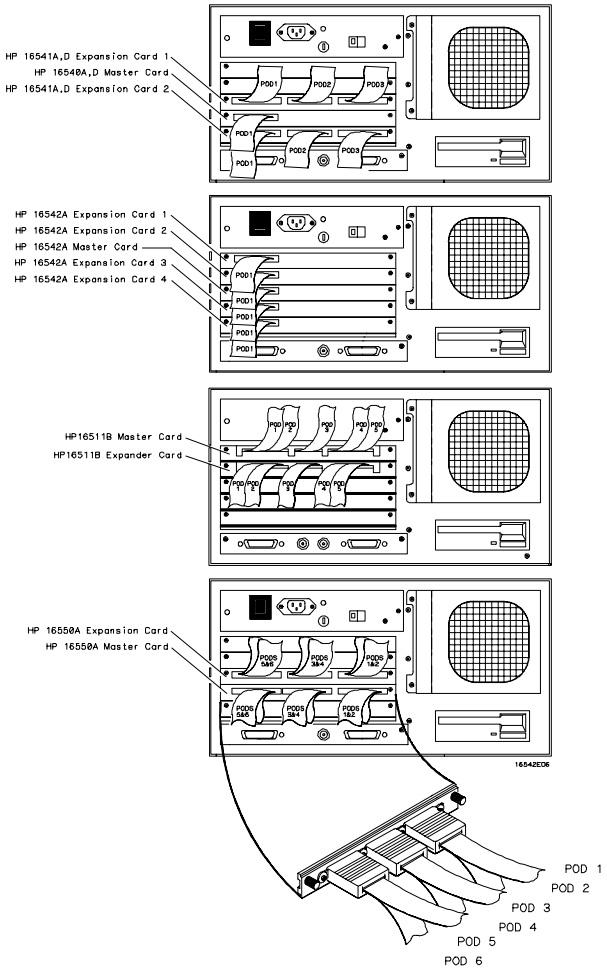

Figure 1-4. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Table 1-1. Logic Analyzer Connections and Configuration Files (State)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B	C186EB_1		*	** P4 (ADDR/ STAT)	P3 (ADDR)	*	P1 J↑ (DATA)
HP 16511B Upper Card	C186EB_3		--	--	--	--	--
HP 16511B Lower Card			*	** P4 (ADDR/ STAT)	P3 (ADDR)	*	P1 J↑ (DATA)
HP 16541A,D Exp. Card 1	C186EB_5				P5 *	** P4 (ADDR/ STAT)	P3 (ADDR)
HP 16540A,D Master Card							P1 J↑ (DATA)
HP 16541A,D Exp. Card 2					P7 *	P6 *	P2 *
HP 16542A Card 1 * **	C186EB_5						P4 **
HP 16542A Master Card							P1 J↑ (DATA)
HP 16542A Card 2 * **							P3 (ADDR)
HP 1660A/61A/62A, HP 16550A	C186EB_7	*	*	** P4 (ADDR/ STAT)	P3 (ADDR)	*	P1 J↑ (DATA)

* P2, P5, P6, P7, and Timing P4 on the preprocessor interface are not required for inverse assembly. They can be connected to any logic analyzer pod marked with an asterisk (*), or left unconnected at the user's discretion. Use GP Probes or termination adapters to monitor these signals (see next section).

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used.

*** For three-card HP 16542A systems, Card 1 is above the Master Card and Card 2 is below the Master Card.

Table 1-2. Logic Analyzer Connections and Configuration Files (Timing)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B	C186EB_2		P7	P6	P5	P4 **	P2
HP 16511B Upper Card	C186EB_4		--	--	--	--	--
HP 16511B Lower Card			P7	P6	P5	P4 **	P2
HP 16541A,D Exp. Card 1	C186EB_6				P5	P4 **	P2
HP 16540A,D Master Card							P6
HP 16541A,D Exp. Card 2					--	--	P7
HP 16542A Card 1 * **	C186EB_6						P4 **
HP 16542A Master Card							P6
HP 16542A Card 2 * **							P7
HP 1660A/61A/62A, HP 16550A	C186EB_8	*	P7****	P6	P5	P4 **	P2

* The timing configuration files are set up for pods P2, P4, P5, P6, and P7. Additional pods can be connected to any logic analyzer pod marked with an asterisk (*), or left unconnected at the user's discretion.

** For timing analysis use only the non-terminated (2 x 10-pin narrow) P4 connector. The signals on P1, P3, and the terminated P4 connectors are latched, and therefore do not provide true timing information.

*** For three-card HP 16542A systems, Card 1 is above the Master Card and Card 2 is below the Master Card. If you use more than three cards, connect P2 to Card 3, and P5 to Card 4.

****For the 1660A only, connect Pod 7 of the analyzer instead of Pod 5.

Connecting the Termination Adapters

The logic analyzer probes must be properly terminated for the logic analyzer to operate correctly. On the preprocessor interface, there are ten connectors. P1, P3, and P4 have both terminated and nonterminated connectors, while P2, P5, P6, and P7 only have nonterminated connectors. You can probe P2, P5, P6, and P7 (and the nonterminated P1, P3, and P4 connectors) with the General Purpose Probes shipped with your logic analyzer or by using 100 kOhm Termination Adapters (HP part number 01650-63203). Note that the terminated and nonterminated P4 connectors contain different signals. The following steps explain how to connect the termination adapters to the preprocessor interface:

1. Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables, and push the termination adapter into the connector.
2. Connect the female end of the termination adapter to the preprocessor interface.
3. Repeat steps 1 and 2 for each termination adapter.

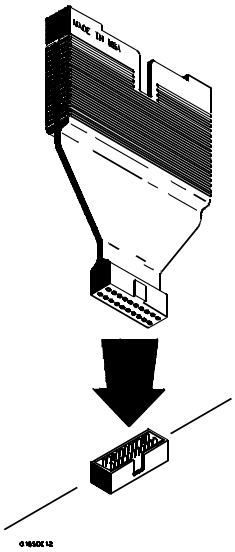

Figure 1-5. Connecting the Termination Adapter

Setting Up the Analyzer from the Disk

The logic analyzer is configured for state analysis by loading the appropriate configuration file. Loading this file also loads a default 16-bit inverse assembler (IA186 or IA186E). To load the configuration and inverse assembler:

1. For the HP 1650A Logic Analyzer, ensure that the HP 1650A system software version is V1.11 or higher.
2. Install the HP E2434B disk in the front disk drive of the logic analyzer.
3. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
   - For HP 16500 and HP 1660 series logic analyzers, select the System Front Disk menu.
4. Configure the menu to "Load" the analyzer with the appropriate state configuration file listed in table 1-1 on page 1-11.
5. For the HP 16500 and HP 1660 series logic analyzers, select the configuration file with the knob, then select "All" and select the correct module or analyzer.
6. Execute the load operation to load the file into the logic analyzer.

The configuration file automatically loads a 16-bit inverse assembler (IA186 or IA186E, see page 2-5). If your target system is an 80C188EB, you must load the 8-bit inverse assembler (IA188). To load the 8-bit inverse assembler, use steps 2 through 6 above, except that for steps 4 and 5 "Load" the inverse assembler instead of the configuration file.

If you have the 8-bit inverse assembler loaded, and store the configuration file to disk (using a different file name), you can later load the new file name, and the 8-bit inverse assembler will automatically load.

Timing Analysis

The HP E2434B can also be used for timing analysis. To configure the logic analyzer for timing analysis, ensure that the timing connections from table 1-2 are made, and load the appropriate timing configuration file from the disk. Use steps 1 through 6 on page 1-14 to load the timing configuration.

Attention! 

The Attention! symbol occurs several places on the labels, and indicates the following items which may be unexpected:

- The signals on the nonterminated (Timing) P1 and P3 connectors are latched. For true timing on the multiplexed Address/Data bus, use P2.
- The DEN signal on P1 (Timing) and P1 (State) has been routed through a delay circuit. Use P5 (Timing) to get DEN as a clock (with no delay), and P4 (Timing) to see true timing on DEN.

Probing With an Oscilloscope

The individual pins on the preprocessor interface can also be probed with an oscilloscope. There are two ground pins on the top of the preprocessor interface (see figure 1-6). Connect the ground lead of the oscilloscope to one of the ground pins on the preprocessor interface, and the other lead to the signal to be measured. The signals are available on the seven non-terminated pods (see top of figure 1-6). Table 3-1 in Chapter 3 lists the correlation between the microprocessor signals, the PGA socket (see figure 3-2), and the connectors.

CLKIN and OSCOUT appear on the 2 x 10 right-angle connector, and can be probed there (see next section).

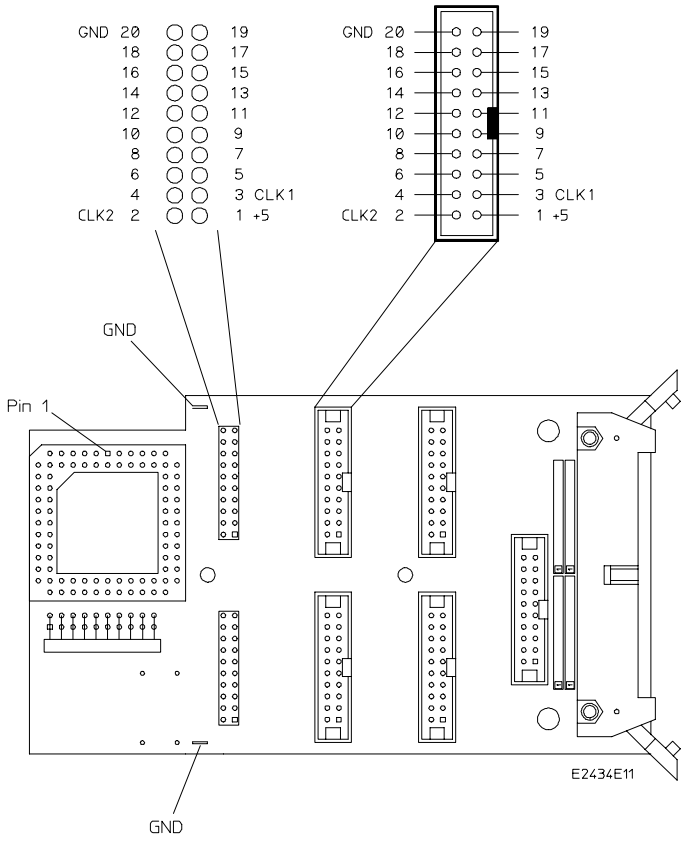

Figure 1-6. Pin Numbers and Ground Pins

Installing an Oscillator or Crystal

In some instances pin protectors will cause loading problems for the target system oscillator or crystal, so that the CLKIN on the microprocessor is not properly driven. A 20-pin right-angle socket on the preprocessor interface (see figure 1-1) allows a crystal to be mounted on the preprocessor interface, for driving the microprocessor. Table 1-3 shows the pinout for the 20-pin right-angle socket. The four pads next to the 2 x 10 right-angle socket on the preprocessor interface are for an oscillator (in place of a crystal).

Three types of configurations are shown in figure 1-7. Configuration A will work for most crystal systems. When used in a third-overtone mode, the tank circuit in configuration B is recommended. Configuration C is for oscillators. See Intel Data Sheet for recommended component values.

To connect a crystal or oscillator, use the following procedure:

1. Remove all power from the preprocessor interface.
2. Remove pins 41 and 40 from the pin protector nearest the preprocessor interface (see page 1-7). This opens the connection from the target system crystal or oscillator to the preprocessor.
3. For crystal configurations, make the connections listed in table 1-4 (configuration A) or 1-5 (configuration B). An HC49U crystal is recommended (for size and shape), that meets Intel's specifications. For Configuration C, solder the oscillator onto the four pads next to the 2 x 10 right-angle socket on the HP E2434B, ensuring that + 5 and GND are correctly aligned. The pads contain traces for the required electrical connections.

Table 1-3. 20-pin Right-angle Socket Pinout

Pin Number	Signal
1 - 10	Ground
11 - 13	Connected to CLKIN
14, 16	no connect
15, 17, 18	Connected to OSCOUT
19, 20	Connected to C3

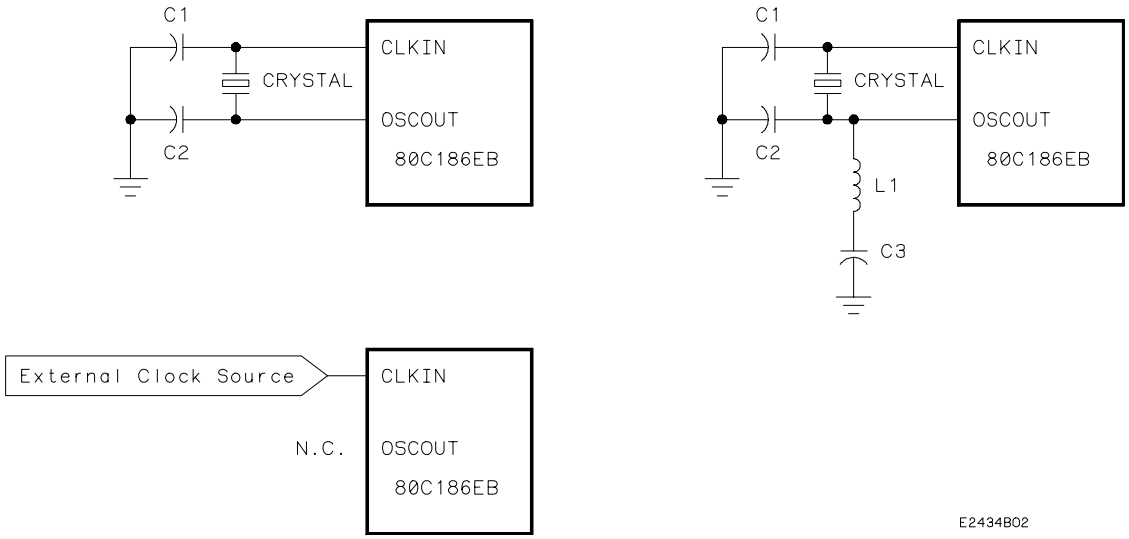

Figure 1-7. Oscillator/Crystal Configurations

Table 1-4. Connections for Configuration A

Pin Numbers	Item Connected
1 and 11 13 and 15 7 and 17	C1 HC49U crystal C2

Table 1-5. Connections for Configuration B

Pin Numbers	Item Connected
1 and 11 13 and 15 7 and 17 18 and 19 10 and 20	C1 HC49U crystal C2 L1 C3

Analyzing the Intel 80C186EB

Introduction

This chapter provides reference information on the format specifications and symbols configured by the HP E2434B software. It also provides information about the inverse assembler and status encoding.

State Format Specification

The 80C186EB Inverse Assembler file contains predefined format specifications (see figure 2-1). These format specifications include all labels for monitoring the 80C186EB microprocessor and any coprocessors connected directly to the microprocessor.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (> 60 ns) for proper HP E2434B operation. For more information on the Clock Period field, refer to your logic analyzer reference manual.

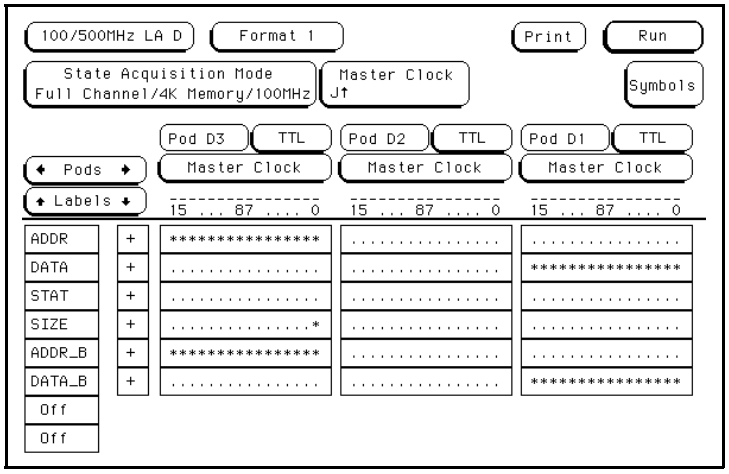

Figure 2-1. State Format Specification

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 2-1 lists the bits assigned to the STAT label. Table 2-2 lists the symbols for the STAT and SIZE labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

Table 2-1. STAT Label Bits

Bit	Status Signals	Description
0 - 2	S0 - S2	These signals indicate the type of cycle the microprocessor is executing.
3	BHE	This signal enables data on the most significant half of the data bus (D15 - D8).
4	GND	This signal is tied low.

Table 2-2. Status Field Encoding

Label	Symbol	Pattern				
		GND	**BHE**	**S2**	**S1**	**S0**
STAT	INT ACK	0	x	0	0	0
	READ IO	0	0	0	0	1
	LB READ IO	0	1	0	0	1
	WRITE IO	0	0	0	1	0
	LB WRITE IO	0	1	0	1	0
	HALT	0	x	0	1	1
	INST FETCH	0	x	1	0	0
	READ MEM	0	0	1	0	1
	LB READ MEM	0	1	1	0	1
	WRITE MEM	0	0	1	1	0
	LB WRITE MEM	0	1	1	1	0
	PASSIVE	0	x	1	1	1
			BHE	**A0**		
SIZE	HIGH BYTE XFER		0	1		
	LOW BYTE XFER		1	0		
	WORD TRANSFER		0	0		
	INVALID STATE		1	1		

Listing Menu

Captured data is displayed as shown in figure 2-2 (with the IA186 inverse assembler) or figure 2-3 (with the IA186E inverse assembler). The inverse assemblers are constructed so the mnemonic output closely resembles the actual assembly source code. In figure 2-3, the unexecuted prefetches have been suppressed.

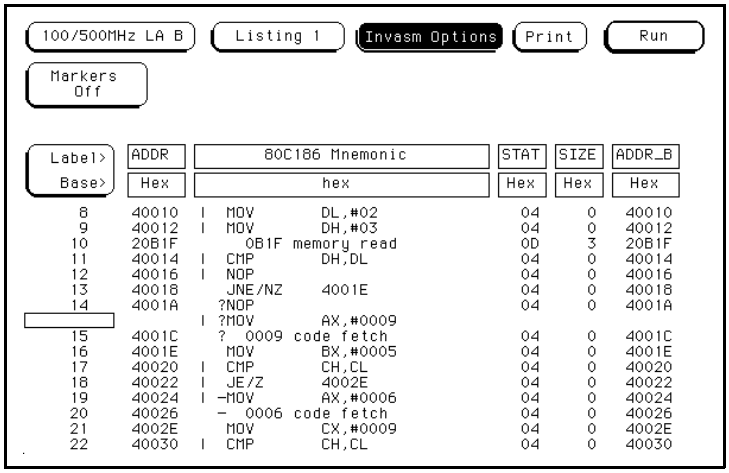

Figure 2-2. State Listing, IA186 Inverse Assembler

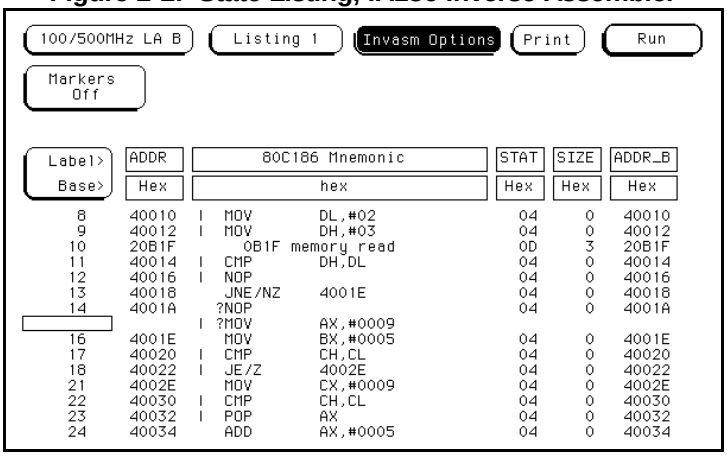

Figure 2-3. State Listing, IA186E Inverse Assembler (Unexecuted Prefetches Suppressed)

The 80C186 Inverse Assemblers

The HP E2434B preprocessor Interface software contains three inverse assemblers. There are two 16-bit inverse assemblers and one 8-bit inverse assembler. The 16-bit inverse assembler with an E suffix (IA186E) is an enhanced version, which contains additional features. The enhanced inverse assembler uses the increased capabilities of the HP 16500B mainframe, or the HP 1660A/61A/62A Logic Analyzers with software version V02.00 or higher. For additional information on the IA186E features, see "The IA186E Inverse Assembler."

Synchronizing the Inverse Assembler

The microprocessor does not provide enough status information to discriminate between the first code fetch cycle of an instruction and subsequent code fetch cycles. You must point to the state that contains the first byte of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

Use the following steps to synchronize the inverse assembler:

1. Identify a line on the display that you know contains the first byte of an opcode fetch.

2. Roll this line to the top of the screen.

Note 

The cursor location is not the top of the display. In figure 2-2, line 8 is at the top of the display.

3. For the IA186 inverse assembler, select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

For the IA186E inverse assembler, select the "Invasm Options" button, and use the "Code Synchronization" portion of the submenu. With the IA186E inverse assembler, also select "Align". The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating steps 1 through 3.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in the hexadecimal format. A lower-case "o" following a numeric value indicates an octal representation (the ESC instruction for example). Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Two instructions may be fetched in a single cycle because the 80C186EB can fetch a word with two instruction bytes from program memory. If the least significant byte of this word contains a single-byte instruction, the next sequential instruction begins in the upper byte. In this case, the two instructions are displayed on two separate lines on the logic analyzer display; the second instruction is prefixed by a vertical bar (|), to indicate that it begins in the upper byte.

Since instructions may begin in either the lower or upper byte, the last byte of a multiple-byte instruction may also occur in the lower byte, with a second instruction beginning in the upper byte. Thus, the following definition: Any instruction prefixed by a vertical bar begins in the upper byte of the fetched word.

Examples:

```
  PUSH DX              (PUSH occupies the lower byte;
| ADC BX,DX            ADC begins in the upper byte.)

  JO     OFLOW_CTL     (JO begins in the lower byte and uses
                        the upper byte as well. Since it is a
                        two-byte instruction, it is displayed on
                        one line.)
```

Pound signs (#) in the inverse assembler output indicate that the numbers following the pound sign (#) are immediate operands.

Asterisks (*) in the inverse assembler output indicate a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

The 80C186EB microprocessor can perform word transfers as well as byte transfers between microprocessor registers and memory. Furthermore, byte transfers may occur on either the upper eight bits or the lower eight bits of the 16-bit data bus. The inverse assembler makes a distinction between these conditions by displaying "xx" (don't care) for the byte of the transfer that was ignored by the microprocessor. In this way, it is possible to determine exactly which byte was used by the microprocessor:

28B3 memory write	(word transfer)
xxB3 memory write	(byte transfer on lower 8 bits)
28xx memory write	(byte transfer on upper 8 bits)

Prefetching Instructions in the Queue (–/?)

The 80C186EB microprocessor is a prefetching microprocessor. That is, it fetches up to three instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and will be discarded by the microprocessor. Unused prefetches are indicated by the prefix "–" in the inverse assembly listing.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most four words, one technique to avoid unwanted triggering from unused prefetches is to add "6" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

On line 18 of figure 2-2, the inverse assembler could determine that the conditional jump was taken to line 21. This was determined when the increment-by-two address sequence was broken. In this case, the inverse assembler prefixed lines 19 and 20 with "–" to indicate that this line was not used.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?" as shown in lines 14 and 15 of figure 2-2.

Instruction Type

The 80C186EB instruction set contains four groups of instructions defining the instruction type in the second opcode byte, rather than in the first byte. In this case, if the second opcode byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These group names are defined as follows:

- Immed - Contains the following instructions when used with immediate source operands:

ADD	AND
OR	SUB
ADC	XOR
SBB	CMP

- Shift - Contains the following logical and arithmetic shifts and rotates:

ROL	SHL/SAL
ROR	SHR
RCL	SAR
RCR	

- Grp_1 - Contains the following instructions:

TEST (see note)	IMUL
NOT	DIV
NEG	IDIV
MUL	

Note

The TEST instruction is included only when the instruction concerns an immediate source operand.

- Grp_2 - Contains the following groups of instructions:

INC	when the instruction concerns memory operands on 8-bit registers.
DEC	when the instruction concerns memory operands on 8-bit registers.
CALL	indirect operand.
JMP	indirect operand.
PUSH	when the instruction concerns 16-bit memory operands.

To reduce the width of the inverse assembler field, LOCK and REPeat prefixes appear on the line before the instruction to which they apply.

Abbreviations

Listed below are several abbreviations for normal programming syntax that have been adopted to reduce the width of the inverse assembler display field.

dwp	- DWORD PTR
wp	- WORD PTR
bp	- BYTE PTR
fp	- FAR PTR
np	- NEAR PTR
s	- SHORT

These symbols are displayed only if the operation size cannot be determined from the instruction itself.

Physical Addresses

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 16-bit intrasegment offset) is displayed instead of a mapped physical address.

Resultant bus cycles must be located in the trace list, so successful address mapping depends on the careful use of storage qualification in the logic analyzer.

Coprocessor Support

The HP E2434B Preprocessor Interface fully supports the 80C187 coprocessor. The 80C187 instructions are inverse assembled and all 80C187 operand transfers are decoded as I/O Reads and Writes.

The IA186E Inverse Assembler

The IA186E (and IA188E) inverse assembler contains additional features which use the increased capabilities of some of the logic analyzers. It supports the HP 16540/16541A,D and HP 16550A Logic Analyzers in the HP 16500B mainframe, and the HP 1660A/61A/62A Logic Analyzers with software version V02.00 or higher. For those logic analyzer systems, the IA186E inverse assembler is automatically loaded when the appropriate configuration file is loaded. Note that all the features in the IA186 inverse assembler are also included in the IA186E inverse assembler (see previous section).

The IA186E Inverse Assembly Options menu contains two functions: display filtering with Show/Suppress selections, and Code Synchronization (see figure 2-4). The following sections describe these functions.

Note

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

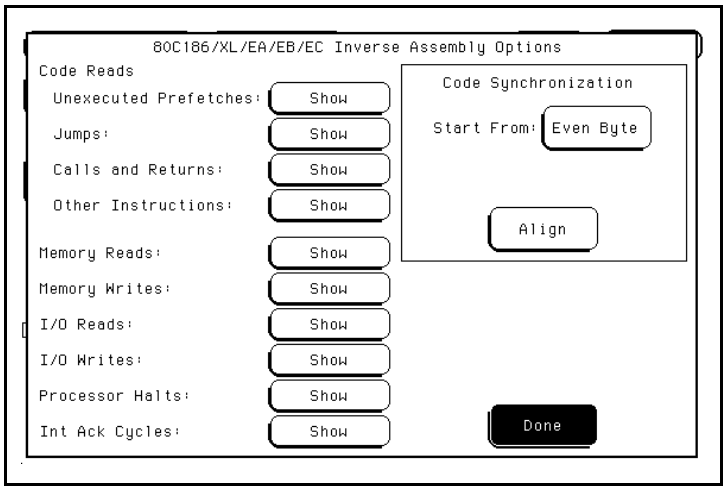

Figure 2-4. IA186E Inverse Assembly Options

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. Figure 2-4 shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Figure 2-4 shows the settings to suppress unexecuted prefetches. Figure 2-3 (page 2-4) shows a listing with the unexecuted prefetches suppressed, so that only executed instructions are displayed. A comparison of figures 2-2 and 2-3 shows the difference in the listing display.

Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To resynchronize the inverse assembler, use the procedure on page 2-5.

Timing Format Specification

When the preprocessor interface is used for timing analysis, the format specification is set up similar to that shown in figure 2-5. The formats may be slightly different, depending on which logic analyzer you are using. The STAT label in the Timing configuration does not contain the GND signal, shown in table 2-2.

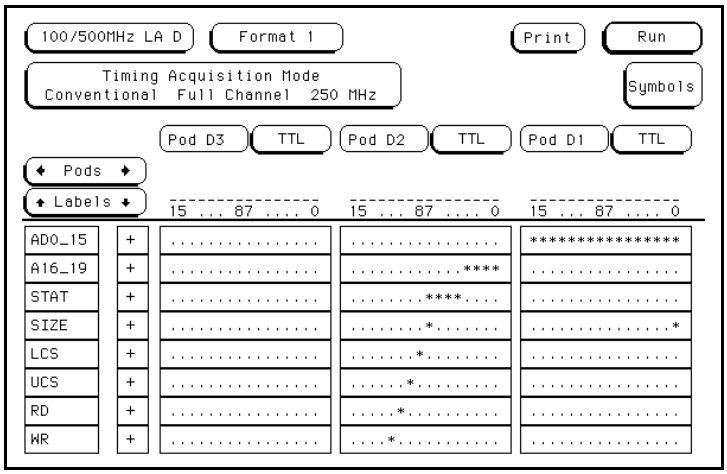

Figure 2-5. Timing Format Specification

Note

In figure 2-5 additional labels are listed offscreen. To view these signals on your logic analyzer, select the Label field and rotate the knob on the front panel clockwise.

Waveforms Display

Captured timing data is displayed in the Waveforms menu as shown in figure 2-6.

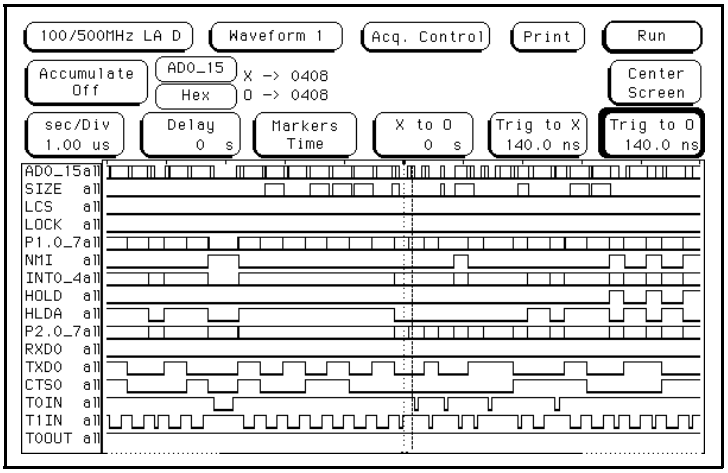

Figure 2-6. 80C186EB Waveforms Display

Note

The value to the right of the field containing AD0_15 is the pattern marked by the X marker. The base of this value is determined by the base of the specified label (AD0_15) that is specified in the timing Trace menu. The "At X (or O) marker" field allows you to select either the X or O marker. The field containing AD0_15 allows you to select any label in the Format menu.

3

General Information

Introduction

This chapter contains the characteristics and signal mapping for the HP E2434B Preprocessor Interface.

HP E2434B Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2434B Preprocessor Interface. These characteristics are included as additional information for the user.

Product Compatibility: Intel 80C186EB and 80C188EB microprocessors (except 80C186EB/188EB PGA), and all microprocessors made by other manufacturers which comply with Intel 80C186EB specifications.

Microprocessor Package: 80-pin QFP and 84-pin PLCC. QFP packages require HP E2434B Option 1CC.

Clock Speed: All clock speeds up to and including 16 MHz, for all supported microprocessors.

Accessories Required: Termination Adapters or GP Probes required for timing analysis. See above for options required for QFP packages.

Signal Line Loading: Approximately 3 pF plus one "FCT" TTL load on AD0-15, A16-19, S0-2, and BHE.
Approximately 3 pF plus one "AS" TTL load on CLKOUT and ALE.
Approximately 3 pF plus one "F" TTL load on AD0-15, NCS, RD, WR, PEREQ, ERROR and DEN.
100 kΩ plus 12 pF on all other lines.

Target Signal Timing: All Data (D0 - D15) must have 4 ns hold with respect to the falling edge of CLKOUT.

Logic Analyzer Required:	HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (master card and one or two expander cards), HP 16542A (three cards), or HP 16550A.	
Number of Probes Used:	Up to eight 16-channel probes.	
Power Requirements:	1.0 A at + 5 Vdc maximum from the logic analyzer.	
Microprocessor Operations Displayed:	Memory Read/Write I/O Read/Write Instruction Fetch Interrupt Acknowledge Halt Transfer to 80C187 coprocessor	
Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches.	
Environmental Temperature:	Operating:	0 to + 55 °C (+ 32 to + 131 °F)
	Nonoperating:	–40 to + 75 °C (–40 to + 167 °F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Clocking

The logic analyzer uses the rising edge of DEN (delayed to ensure proper setup and hold for the logic analyzer) to clock information into the logic analyzer.

Interface Design

The primary function of a preprocessor interface is to connect the target microprocessor to the logic analyzer, and to perform any functions unique to that particular microprocessor. The HP E2434B Preprocessor Interface performs this primary function by latching and buffering the address, status, and data of the microprocessor so that address, status, and data can be sent to the logic analyzer at the same time (see figure 3-1).

The multiplexed Address/Data bus is demultiplexed by the preprocessor interface. The address and status latches are clocked with an inverted version of ALE. The data latches are clocked with an inverted version of the microprocessor CLKOUT.

The logic analyzer uses the rising edge of DEN (delayed to ensure proper setup and hold for the logic analyzer) to clock information into the logic analyzer.

All signals can be probed on the non-terminated pods. The signals on these pods are routed straight through from the microprocessor, with no active circuitry in between.

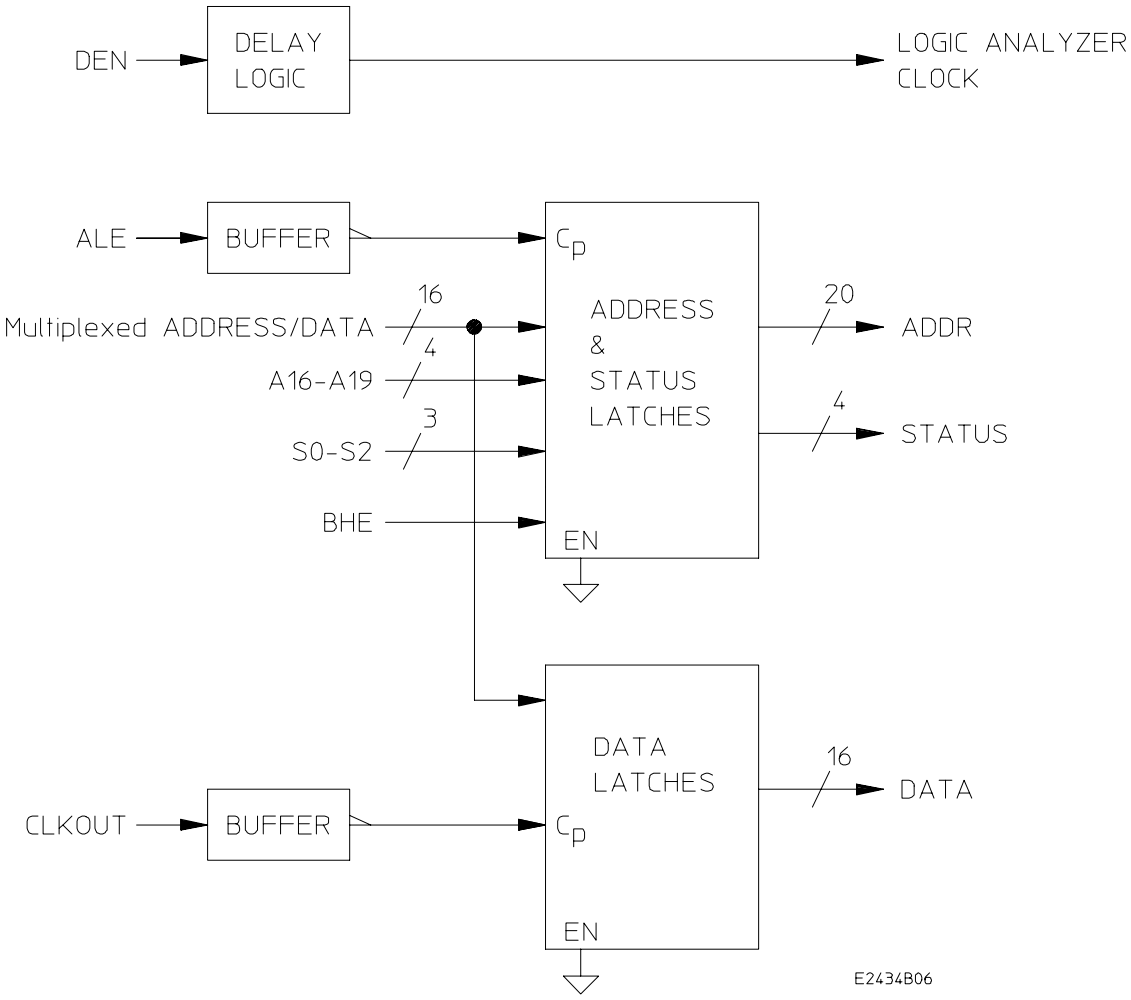

Figure 3-1. HP E2434B Block Diagram

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2434B Preprocessor Interface. Since the pods on the logic analyzers are numbered differently than the pods on the preprocessor interface, refer to table 1-1 or 1-2 to correlate the pod numbers to your logic analyzer.

If there is no state or timing designation after the connector number in table 3-1, the preprocessor interface pin number refers to the non-terminated (2 x 10) connector pins.

Figure 3-2 shows the top view of the PGA pattern on the preprocessor interface, with the PLCC pin numbers marked.

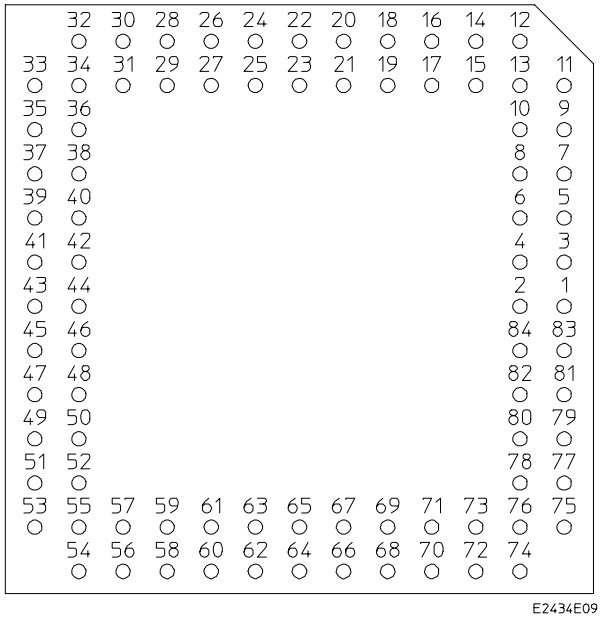

Figure 3-2. PGA to PLCC Pin Mapping (Top View)

Table 3-1. Signal-to-Connector List

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P3 / 19	0	61 *	10 *	A0	ADDR
P3 / 18	1	66 *	15 *	A1	ADDR
P3 / 17	2	68 *	17 *	A2	ADDR
P3 / 16	3	70 *	19 *	A3	ADDR
P3 / 15	4	72 *	21 *	A4	ADDR
P3 / 14	5	74 *	23 *	A5	ADDR
P3 / 13	6	76 *	25 *	A6	ADDR
P3 / 12	7	78 *	27 *	A7	ADDR
P3 / 11	8	62 *	11 *	A8	ADDR
P3 / 10	9	67 *	16 *	A9	ADDR
P3 / 9	10	69 *	18 *	A10	ADDR
P3 / 8	11	71 *	20 *	A11	ADDR
P3 / 7	12	73 *	22 *	A12	ADDR
P3 / 6	13	75 *	24 *	A13	ADDR
P3 / 5	14	77 *	26 *	A14	ADDR
P3 / 4	15	79 *	28 *	A15	ADDR
P4 / 19 (timing)	0	80	29	A16	(note 1)
P4 / 18 (timing)	1	81	30	A17	(note 1)
P4 / 17 (timing)	2	82	31	A18	(note 1)
P4 / 16 (timing)	3	83	32	A19 / ONCE	(note 1)
P4 / 15 (timing)	4	10	42	S0	(note 1)
P4 / 14 (timing)	5	9	41	S1	(note 1)
P4 / 13 (timing)	6	8	40	S2	(note 1)
P4 / 12 (timing)	7	7	39	BHE	(note 1)

* These pin numbers refer to the multiplexed Address/Data Bus. The signal on the preprocessor interface is either the latched address or the latched data information.

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P4 / 11 (timing)	8	29	60	LCS	(note 1)
P4 / 10 (timing)	9	30	61	UCS	(note 1)
P4 / 9 (timing)	10	4	36	RD	(note 1)
P4 / 8 (timing)	11	5	37	WR	(note 1)
P4 / 7 (timing)	12	6	38	ALE	(note 1)
P4 / 6 (timing)	13	16	--	DT/R	(note 1)
P4 / 5 (timing)	14	11	43	DEN	(note 1)
P4 / 4 (timing)	15	15	47	LOCK	(note 1)
P4 / 37 (state)	0	80	29	A16	ADDR
P4 / 35 (state)	1	81	30	A17	ADDR
P4 / 33 (state)	2	82	31	A18	ADDR
P4 / 31 (state)	3	83	32	A19	ADDR
P4 / 29 (state)	4	10	42	S0	STAT
P4 / 27 (state)	5	9	41	S1	STAT
P4 / 25 (state)	6	8	40	S2	STAT
P4 / 23 (state)	7	7	39	BHE	STAT
P4 / 21 (state)	8	--	--	Gnd	STAT
P4 / 19 (state)	9	66 *	15	A1	(note 2)
P4 / 17 (state)	10	68 *	17	A2	(note 2)
P4 / 15 (state)	11	5	37	WR	(note 2)
P4 / 13 (state)	12	4	36	RD	(note 2)
P4 / 11 (state)	13	60	--	NCS	(note 2)
P4 / 9 (state)	14	39	--	PEREQ	(note 2)
P4 / 7 (state)	15	3	--	ERROR	(note 2)

* These pin numbers refer to the multiplexed Address/Data Bus. The signal on the preprocessor interface is either the latched address or the latched data information.

Note 2. These signals are latched; they are not used for inverse assembly.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P1 / 19	0	61 *	10 *	D0	DATA
P1 / 18	1	66 *	15 *	D1	DATA
P1 / 17	2	68 *	17 *	D2	DATA
P1 / 16	3	70 *	19 *	D3	DATA
P1 / 15	4	72 *	21 *	D4	DATA
P1 / 14	5	74 *	23 *	D5	DATA
P1 / 13	6	76 *	25 *	D6	DATA
P1 / 12	7	78 *	27 *	D7	DATA
P1 / 11	8	62 *	11 *	D8	DATA
P1 / 10	9	67 *	16 *	D9	DATA
P1 / 9	10	69 *	18 *	D10	DATA
P1 / 8	11	71 *	20 *	D11	DATA
P1 / 7	12	73 *	22 *	D12	DATA
P1 / 6	13	75 *	24 *	D13	DATA
P1 / 5	14	77 *	26 *	D14	DATA
P1 / 4	15	79 *	28 *	D15	DATA
P2 / 19	0	61	10	AD0	(note 1)
P2 / 18	1	66	15	AD1	(note 1)
P2 / 17	2	68	17	AD2	(note 1)
P2 / 16	3	70	19	AD3	(note 1)
P2 / 15	4	72	21	AD4	(note 1)
P2 / 14	5	74	23	AD5	(note 1)
P2 / 13	6	76	25	AD6	(note 1)
P2 / 12	7	78	27	AD7	(note 1)

* These pin numbers refer to the multiplexed Address/Data Bus.
Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P2 / 11	8	62	11	AD8	(note 1)
P2 / 10	9	67	16	AD9	(note 1)
P2 / 9	10	69	18	AD10	(note 1)
P2 / 8	11	71	20	AD11	(note 1)
P2 / 7	12	73	22	AD12	(note 1)
P2 / 6	13	75	24	AD13	(note 1)
P2 / 5	14	77	26	AD14	(note 1)
P2 / 4	15	79	28	AD15	(note 1)
P5 / 19	0	28	59	P1.0 / GCS0	(note 1)
P5 / 18	1	27	58	P1.1 / GCS1	(note 1)
P5 / 17	2	26	57	P1.2 / GCS2	(note 1)
P5 / 16	3	25	56	P1.3 / GCS3	(note 1)
P5 / 15	4	24	55	P1.4 / GCS4	(note 1)
P5 / 14	5	21	52	P1.5 / GCS5	(note 1)
P5 / 13	6	20	51	P1.6 / GCS6	(note 1)
P5 / 12	7	19	50	P1.7 / GCS7	(note 1)
P5 / 11	8	17	48	NMI	(note 1)
P5 / 10	9	31	62	INT0	(note 1)
P5 / 9	10	32	63	INT1	(note 1)
P5 / 8	11	33	64	INT2 / INTA0	(note 1)
P5 / 7	12	34	65	INT3 / INTA1	(note 1)
P5 / 6	13	35	66	INT4	(note 1)
P5 / 5	14	13	45	HOLD	(note 1)
P5 / 4	15	12	44	HLDA	(note 1)

Note 1. These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P6 / 19	0	57	7	P2.0 / RXD1	(note 1)
P6 / 18	1	58	8	P2.1 / TXD1	(note 1)
P6 / 17	2	59	9	P2.2 / BCLK1	(note 1)
P6 / 16	3	55	5	P2.3 / SINT1	(note 1)
P6 / 15	4	56	6	P2.4 / CTS1	(note 1)
P6 / 14	5	54	4	P2.5 / BCLK0	(note 1)
P6 / 13	6	50	80	P2.6	(note 1)
P6 / 12	7	49	79	P2.7	(note 1)
P6 / 11	8	53	3	RXD0	(note 1)
P6 / 10	9	52	2	TXD0	(note 1)
P6 / 9	10	51	1	CTS0	(note 1)
P6 / 8	11	46	76	T0IN	(note 1)
P6 / 7	12	48	78	T1IN	(note 1)
P6 / 6	13	45	75	T0OUT	(note 1)
P6 / 5	14	47	77	T1OUT	(note 1)
P6 / 4	15	18	49	READY	(note 1)
P7 / 18	1	44	74	CLKOUT	(note 1)
P7 / 16	3	38	69	RESOUT	(note 1)
P7 / 14	5	37	68	RESIN	(note 1)
P7 / 12	7	36	67	PDTMR	(note 1)
P7 / 10	9	14	46	TEST / BUSY	(note 1)
P7 / 8	11	60	--	NCS	(note 1)
P7 / 6	13	3	--	ERROR	(note 1)
P7 / 4	15	39	--	PEREQ	(note 1)

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EB Pin PLCC	80C186EB Pin QFP	Pin Mnemonic	Label
P1 / 3	CLK	11	43	DEN *	J CLOCK
P2 / 3	CLK	6	38	ALE	
P5 / 3	CLK	11	43	DEN	
P6 / 3	CLK	44	74	CLKOUT	

* This is a delayed version of DEN.

Servicing

The repair strategy for the HP E2434B is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2413-66504	Interface Circuit Board
E2434-66502	Personality Circuit Board
E2434-68705	Inverse Assembler Disk Pouch
1200-1744	84-pin Pin Protector

Dimensions

Figure 3-3 lists the dimensions for the HP E2434B circuit board. The dimensions are listed in inches / millimeters.

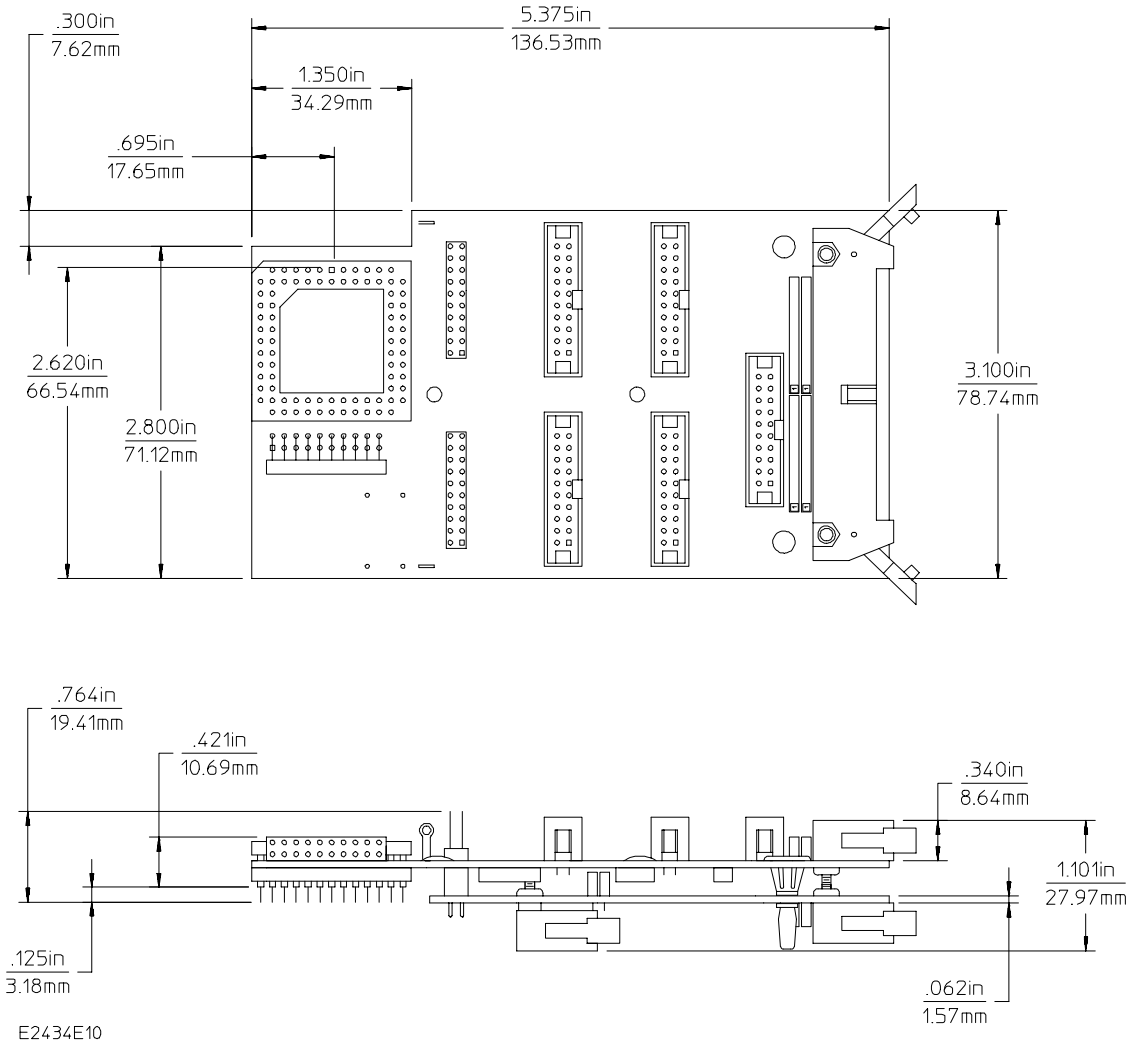

Figure 3-3. HP E2434B Dimensions – inches / mm

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface are not installed properly, or they are not making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501A,B frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A,B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading an appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers, if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If a passive preprocessor interface is available, try using that instead of an active one.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded"

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16542A or HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.